AMENDMENTS TO THE CLAIMS

Following is a listing of the claims, which will replace all prior versions and listings of claims in this application:

Listing of the Claims

1. (Canceled)

2. (Currently Amended) A ~~The~~ memory circuit, ~~according to claim 1,~~ comprising:

a memory cell array including a plurality of bit lines, a plurality of word lines, and a plurality of memory cells disposed in positions of intersection between the bit lines and the word lines; and

a page buffer, which is connected to the bit line and which detects memory cell data by judging with predetermined sense timing a potential of the bit line when a pre-charged bit line potential is discharged in accordance to a cell current of a selected memory cell, wherein the sense timing differs in accordance with a position of the selected memory cell in the memory cell array, and

wherein, when the selected memory cell is positioned at a first distance from the page buffer, the page buffer makes a judgment by means of first sense timing, and when the selected memory cell is positioned at a second distance from the page buffer which is longer than the first distance, the page buffer makes a judgment by means of second sense timing that lags behind the first sense timing.

3. (Currently Amended) The memory circuit according to claim ~~1~~ 2, wherein, when the selected memory cell is positioned at a first distance from a word line driver circuit for driving the word lines, the page buffer makes a judgment by means of first sense timing, and when the selected memory cell is positioned at a second distance from the word line driver circuit which is longer than the first distance, the page buffer makes a judgment by means of second sense timing that lags behind the first sense timing.

4. (Currently Amended) The memory circuit according to claim ~~1~~ 2, further comprising:

a delay circuit for generating a sense timing signal by delaying a reference sense timing signal by a delay interval that depends on an address that specifies the position of the selected memory cell, wherein the page buffer detects the potential of the corresponding bit line in response to the sense timing signal supplied by the delay circuit.

5. (Original) A memory circuit, comprising: an ordinary memory cell array including a plurality of bit lines, a plurality of word lines, and a plurality of memory cells disposed in positions of intersection between the bit lines and the word lines; a page buffer, which is connected to the bit line and which detects memory cell data by judging with predetermined sense timing a potential of the bit line when a pre-charged bit line potential is discharged in accordance to a cell current of a selected memory cell; and a reference memory cell array including

reference bit line, and reference memory cells disposed in positions of intersection between the reference bit line and the word lines, wherein the sense timing of the page buffer is determined in accordance with a potential of the reference bit line which is discharged by cell currents of the reference memory cells that belong to a selected word line.

6. (Original) The memory circuit according to claim 5, wherein the reference bit line is disposed in position further from the word line driver circuit for driving the word lines than the ordinary memory cell array.

7. (Original) The memory circuit according to claim 5, wherein threshold voltages of the reference memory cells are set such that the reference bit line discharge produced by the reference memory cells lags behind the bit line discharge produced by ordinary memory cells in an erased state.

8. (Original) The memory cell according to claim 5, wherein threshold voltages of the reference memory cells are set at the highest level among levels for which the reference memory cells are judged as being in an erased state.

9. (Original) The memory circuit according to claim 5, wherein the reference memory cells and the reference bit line include at least reference memory cells and a reference bit line for a read operation as well as reference memory cells and a reference bit line for a program verify operation; and

threshold voltages of the program verify reference memory cells are set such that the reference bit line discharge produced by the program verify reference memory cells lags behind the bit line discharge produced by memory cells that are ordinary memory cells and not in a programmed state.

10. (Original) The memory circuit according to claim 5, wherein the reference memory cells and the reference bit line include at least reference memory cells and a reference bit line for a read operation as well as reference memory cells and a reference bit line for a program verify operation; and threshold voltages of the program verify reference memory cells are set at the highest level among levels for which the program verify reference memory cells are judged as being in an unprogrammed state during a program verify operation.

11. (Original) A memory circuit, comprising: a memory cell array including a plurality of bit lines, a plurality of word lines, and a plurality of memory cells disposed in positions of intersection between the bit lines and the word lines; and a page buffer, which is connected to the bit line and which detects memory cell data by judging with predetermined sense timing a potential of the bit line when a pre-charged bit line potential is discharged in accordance to a cell current of a selected memory cell, wherein the memory cell array is divided into a plurality of regions in the word line direction, and the divided regions include a reference bit line and reference memory cells disposed in positions of

intersection between the reference bit line and the word lines; and the respective sense timing of the page buffers that belong to the divided regions is determined in accordance with a potential of the reference bit line which is discharged by cell currents of reference memory cells connected to a selected word line, in the corresponding divided regions.

12. (Original) The memory circuit according to claim 11, wherein the reference bit lines in the divided regions are disposed in a position further from the word line driver circuit for driving the word lines than the ordinary memory cell array in each divided region.

13. (Original) The memory circuit according to claim 11, wherein threshold voltages of the reference memory cells are set such that the reference bit line discharge produced by the reference memory cells lags behind the bit line discharge produced by ordinary memory cells in an erased state.

14. (Original) The memory circuit according to claim 11, wherein the reference memory cells and the reference bit line include at least reference memory cells and a reference bit line for a read operation as well as reference memory cells and a reference bit line for a program verify operation; and threshold voltages of the program verify reference memory cells are set such that the reference bit line discharge produced by the program verify reference

memory cells lags behind the bit line discharge produced by memory cells that are ordinary memory cells and not in a programmed state.